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Pentacene thin-film transistors with polymeric gate dielectric

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Abstract

Pentacene thin-film transistors have been obtained using polymethyl methacrylate as a gate dielectric. The maximum process temperature was 170 °C, which corresponds to the baking of the polymeric gate dielectric. These devices presented good electrical performances with field-effect mobilities of 0.01 $cm^2 V^{-1} s^{-1}$ and low threshold voltages (−15 V). Atomic force microscopy studies reveal that the microstructure of pentacene layers is strongly conditioned by the surface morphology of the dielectric.

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1. Introduction

The performance of organic thin-film transistors (OTFT) using small molecules has considerably improved during the last years. Organic materials have the key advantage of potentially simple and low-temperature thin-film processing, using techniques as spin coating, ink jet printing or stamping. This fact suggests that OTFTs could be competitive for applications requiring large-area coverage, low-temperature processing and low cost. Such applications include large area sensor and display applications, as well as low-cost application-specific integrated circuits (ASICs).

Among thin-film transistors (TFTs) with an organic semiconductor as the active channel, those fabricated with pentacene have allowed the highest performance. Mobilities up to 1.5 $cm^2 V^{-1} s^{-1}$ and threshold voltages comparables to those obtained with hydrogenated amorphous silicon have been reported by several laboratories [1,2].

The most usual gate dielectric in these pentacene devices is thermally grown silicon dioxide on crystalline silicon. However, for large area applications the use of inorganic dielectrics grown at high temperatures is not of particular interest. The use of organic or polymeric materials which can be spin cast or dip coated are more attractive.

Although polymeric insulators are used in the electronic industry as packaging of chips, silicon

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dioxide is the usual dielectric incorporated on-chip throughout the industry. Actually, very few attempts to substitute silicon dioxide with polymers have been reported to date. Dimitrakopoulos et al. [3] have studied the use of amorphous mixed metal oxide insulators with high dielectric constants as a gate dielectric material on field-effect structures. Using barium zirconate titanate ($\varepsilon = 17.3$) and barium strontium titanate ($\varepsilon = 16$) these authors fabricated pentacene TFTs with good electrical performance. They have also reported that the use of relatively high dielectric insulators allows the obtention of pentacene TFTs with high mobility and low operating voltages. Knipp et al. [4] have recently reported the use of organic materials with low dielectric constants ($\varepsilon = 2.5$–2.6) such as benzocyclobutene or poly-vinyl phenol as a gate dielectric to fabricate pentacene TFTs with electrical performances similar to those obtained using inorganic dielectrics (such as thermal silicon dioxide and silicon nitride by plasma-enhanced CVD). The use of poly-vinyl phenol as a dielectric was also tested by Sirringhaus [5].

In this paper we present the electrical characteristics of pentacene thin-film transistors using polymethyl methacrylate (PMMA) as the gate dielectric material. PMMA is a polymeric resist commonly used in high resolution nanolithographic processes which use electron beam, deep UV (220–250 nm) or X-ray radiation. PMMA has been also used as a protective layer for wafer thinning. Its thermal and mechanical stability, together with a high resistivity ($>2\times10^{15}$ Ω cm) and suitable dielectric constant, similar to that of silicon dioxide ($\varepsilon = 2.6$ at 1 MHz, $\varepsilon = 3.9$ at 60 Hz), make PMMA a good candidate as a dielectric layer in MIS (metal-insulator-semiconductor) structures. Besides, PMMA can be easily deposited on large areas by spin-coating and baked at low temperatures (<170 °C).

2. Experimental

The TFT device structure used in this study is shown in Fig. 1. We have used crystalline silicon as a substrate because of its flatness. Before the deposition of the dielectric film, a chromium layer was thermally evaporated to form the gate electrode.

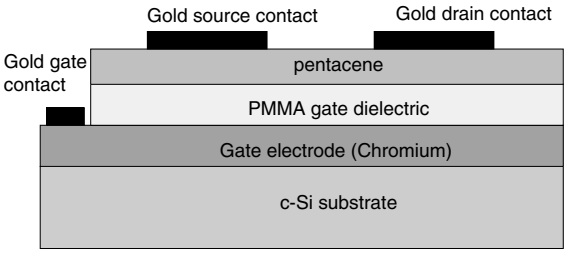

Fig. 1. Schematic cross-section of a pentacene thin-film transistor. The width of the channel was 600 μm, its length 120 μm, and the thickness of the PMMA gate dielectric was 700 nm.

As purchased PMMA [6] with a molecular weight of 950 K diluted in anisole (5%) was used. The resist was spun at 4000 rpm for 40 s to form an uniform coating. Finally the resist was baked at 170 °C for 30 min in a conventional oven. The PMMA thickness was 700 nm as determined by surface profilometry.

Pentacene (Aldrich 97%), without further purification, was deposited at room temperature by thermal evaporation in a high-vacuum system with a base pressure of 1×10^{-6} mbar [7]. No optimization of the technological parameters used to deposit the pentacene films has been carried out yet. To define and isolate the devices pentacene was evaporated through a metallic mask. The thickness of the pentacene layer was about 800 nm, which corresponds to a deposition rate of 25 Å/s. Finally, gold contacts were thermally evaporated through a shadow mask to form the drain and source electrodes. These devices had a channel length of 120 μm and a width of 600 μm.

We did not perform any modification of the surface dielectrics. It has been reported that the electrical characteristics of pentacene TFTs can be improved by using a self-organizing material between gate dielectrics and the pentacene active layer [8].

The electrical characterization of TFTs was made at room temperature using a Hewlett-Packard 4145B semiconductor parameter analyzer. All measurements were made without vacuum and no precautions were taken to prevent the degradation of pentacene films.

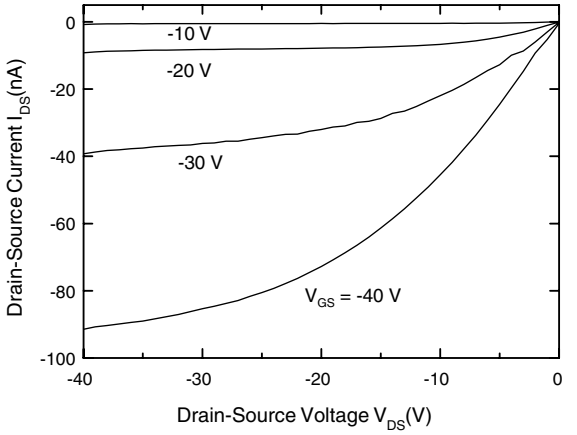

Fig. 2. Drain–source current as a function of the drain–source voltage for several values of the gate–source voltage.

Fig. 2 shows the output characteristic, i.e., the drain–source current (I_{DS}) as a function of drain–source voltage (V_{DS}) for different gate–source voltages (V_{GS}). The conductance values at low drain–source voltage are initially high, and decrease with increasing drain–source voltage, indicating a good ohmic contact between pentacene and both source and drain electrodes.

Fig. 3 shows the I_{DS} plotted on a log scale as a function of V_{GS} for a V_{DS} of −40 V (transfer characteristic). The device exhibits an excellent p-type semiconductor like characteristic. For negative gate–source voltages the device operates in the accumulation mode (hole accumulation). When the gate is positively biased the channel interface is depleted of carriers and the device operates in the depletion mode. It has been reported [9] that evaporated pentacene films usually form an accumulation channel at the gate interface and a positive voltage is necessary to deplete the channel. In this situation the device is normally "on" and current leakages could be significant. In our case, devices are "off" for zero applied gate–source voltages. We attribute this behaviour to the different properties of pentacene films grown on PMMA.

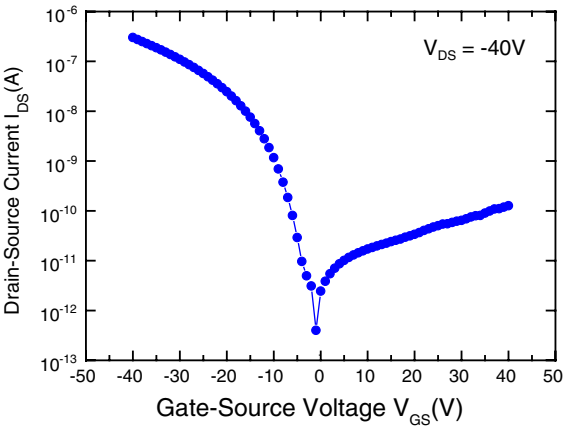

Fig. 3. Drain–source current plotted on a log scale as a function of the gate–source voltage. The drain–source voltage was −40 V. The I_{ON}/I_{OFF} ratio from −20 to 20 V was over 10^3.

From Fig. 3 we calculate that the ratio of the current in the accumulation region to the current in the depletion region (I_{ON}/I_{OFF}) is about 10^3 for our devices (when V_{GS} changes from −20 to 20 V). The devices show a subthreshold slope of about 2.1 V/decade at $V_{DS} = -5$ V.

In Fig. 4 we plot $|I_{DS}|^{1/2}$ versus V_{GS} in the saturation regime ($V_{GS} = V_{DS}$). A saturation field-effect mobility near 0.01 $cm^2/V\,s$ and a threshold voltage V_T near −15 V was obtained. The measured field effect mobility is in agreement with reported hole mobilities from evaporated pentacene thin-film field effect structures [10]. It is interesting to point out that the TFTs have a negative threshold

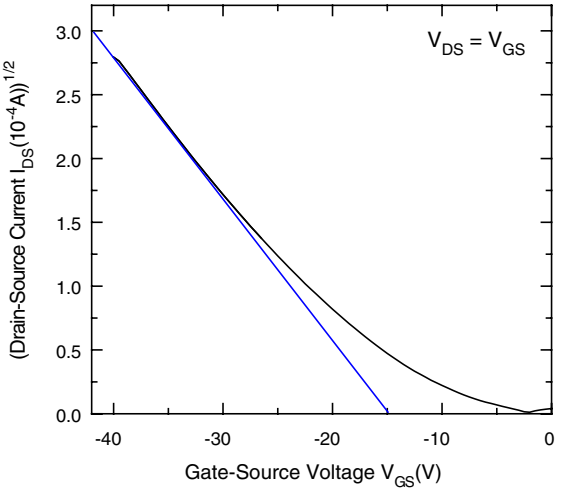

Fig. 4. Square-root of the drain–source current as a function of the drain–source voltage measured in the saturation region (i.e. $V_{GS} = V_{DS}$). The fit allows to calculate a field effect mobility of 0.01 $cm^2/V\,s$ and a threshold voltage −15 V.

voltage. This makes it easier to implement integrated circuits.

On the other hand, we have also fabricated pentacene TFTs following an identical process to that described above, but using silicon dioxide as a gate dielectric material. This silicon dioxide was thermally grown at 1100 °C on the crystalline silicon wafer with a thickness of 200 nm. The silicon dioxide based pentacene TFTs presented poor electrical characteristics, with field-effect mobilities rather measurable.

3. Discussion

Pentacene thin-films obtained by a thermal evaporation process usually present a polycrystalline structure composed by crystalline grains of different shape and size, as can be seen from scanning electron microscopy and X-ray diffraction measurements [7]. While carrier mobility within a crystal grain is high, in polycrystalline structures grain boundaries scatter the carriers, resulting in lower mobilities.

In order to achieve a higher carrier mobility, it would be necessary to reduce the number of grain boundaries, i.e., the number of crystalline grains per unit area. Bigger crystalline grains can be acomplished by a prior purification of the pentacene material (sublimation purification), or by adjusting the deposition parameters. It has been reported that deposition at moderate temperatures (60 °C) and low deposition rates (around 1 Å/s) allow the obtention of pentacene thin-films with higher crystallinity.

Another way to increase the crystallinity is based on the modification of the dielectric surface by chemically processing the gate insulator. This strategy rely on the phenomenon that the size of pentacene crystal grains seems to be strongly dependent on the interface with the material under the deposited film [11]. Apparently, the pentacene crystalline grains grow around a core of impurities in the dielectric film surface. Thus, the chemical modification of the surface allows processing higher pentacene grains. A monolayer of organic cyclohexene coated over the gate dielectric is usually used to obtain bigger crystalline grains [8].

In order to investigate the influence of the PMMA surface on the estructural properties of pentacene layers, we have performed atomic force microscopy analysis of the pentacene films deposited on PMMA and on silicon dioxide. In Fig. 5 we show the topographic image of the pentacene film deposited on PMMA. It can be observed that the pentacene film shows a granular microstructure with an rms roughness around 70 nm. In Fig. 6 we

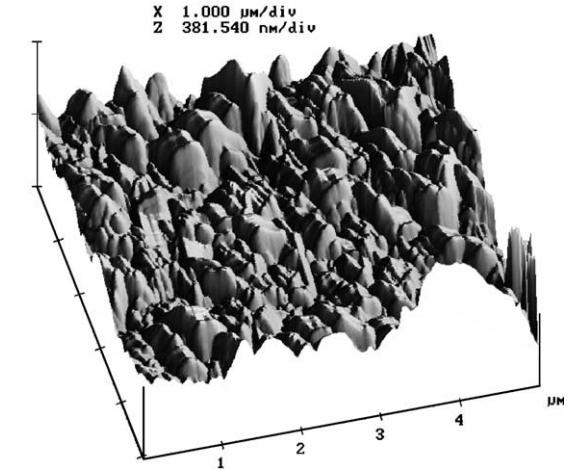

Fig. 5. Pentacene thin-film layer deposited on PMMA polymer dielectric.

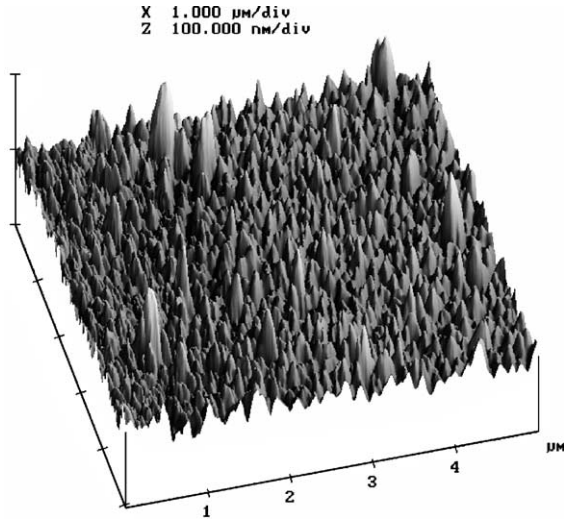

Fig. 6. Pentacene thin-film layer deposited on thermal silicon dioxide dielectric.

observe that pentacene layers grown on silicon dioxide show an structure with much smaller granullar sizes. Summarizing, we consider that the PMMA surface could favour the obtention of bigger crystalline grains, which consequently leads to improved field-effect mobilities.

Nevertheless, further research should be done to optimize the pentacene evaporation parameters (substrate temperature, deposition rate) and of the PMMA processing (solvent, spin speed, bake) in order to establish a correlation between pentacene grain size and field-effect mobility.

4. Conclusions

The results presented in this work show that PMMA can be used as a gate dielectric for pentacene thin-film transistors. This polymeric dielectric can be deposited easily by spin coating. The maximum temperature in the whole device manufacturing process was 170 °C, corresponding to the PMMA baking. The fabricated devices, without any optimization of the pentacene evaporation process, present good electrical performance, with mobilities around 0.01 $cm^2 V^{-1} s^{-1}$ and low threshold voltages (−15 V). PMMA seems to influence the pentacene thin-film microstructure, increasing the crystallinity which results in a higher field effect mobility of TFTs.

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